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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PEUGH, BRIAN R	

ART UNIT	PAPER NUMBER
2187	15

DATE MAILED: 04/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/641,519	RYAN, KEVIN J.	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-23 and 26-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-7,13,14,17-19,22,23,26-29,35,36,39-41,44-46,49-51 and 54-58* is/are rejected.

7)☒ Claim(s) *8-12,15,16,20,21,30-34,37,38,42,43,47,48,52 and 53* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office Action is in response to applicant's communication filed February 17, 2004 in response to PTO Office Action dated November 14, 2003 The applicant's remarks and amendment to the specification and/or claims were considered with the results that follow.

Claims 1, 4-23, and 26-58 have been presented for examination in this application. In response to the last Office Action, claims 1, 13, 23, 35, 45, and 55-58.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-7, 13, 14, 17-19, 22, 23, 26-29, 35, 36, 39-41, 44-46, 49-51, and 54-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al. (US# 5,999,474) and Nakajima (US# 4,807,289).

Regarding claims 1 and 55, Leung et al. teaches a DRAM including memory cells (col. 2, lines 28-29). Leung et al. further teaches determining that a refresh cycle is

required according to the RFQ# signal being asserted low at the beginning of clock cycles T3 and T5 (Fig. 3). Command access B(N) and D(P) occur at the same time as the refresh cycles, where T3 or T5 may be seen as the first predetermined time slot, since this is when the command and refresh arbitration will begin. The refresh will occur concurrently with the access request as long as the request does not result in a cache miss (col. 10, lines 60-66; col. 12, lines 27-39). The second predetermined time slot may be attributed to a time slot after all command accesses have occurred, such as any time after the command D(P).

The difference between the claimed subject matter and that of Leung et al., disclosed supra, is that claims 1 and 55 recite that the first and second predetermined slots are the only time slots during which data access commands may be placed on the bus. Nakajima teaches a system for assigning refresh cycles and memory access cycles according to a designated pattern every refresh cycle (Figure 2; col. 3, lines 15-19 & 31-35). Nakajima also teaches that the data access may be provided every second or third refresh cycle (Figure 3; col. 3, lines 40-47).

Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Leung et al. and Nakajima before him at the time the invention was made to modify the refresh system of Leung et al. to include the access scheduling of Nakajima, because then a computing system incorporating a slower bit rate of 32K bit/sec can be carried out by providing a data access every other refresh cycle, as taught by Nakajima (col. 3, lines 40-44).

Regarding claim 4 and 5, Leung et al. teaches that should a cache miss not occur, then it has been determined that the command access will not conflict with the refresh, as previously recited above, and that the refresh is allowed to occur.

Regarding claims 6 and 7, Leung et al. teaches that when the access command results in a cache miss at the same time of a refresh operation (T5), the access command is allowed to proceed while all DRAM banks except for the DRAM bank corresponding to the command access are allowed to refresh. After the access command has occurred, with the read and write request signals de-asserted high at cycle T6, the refresh command for the DRAM bank related to the access command is allowed to occur at this time (col. 13, lines 26-37, 43-50 and line 62 – col. 14, line 10).

Regarding claims 13, 23, and 56, Leung et al. teaches a DRAM including memory cells (col. 2, lines 28-29). Leung et al. further teaches determining that a refresh cycle is required according to the RFQ# signal being asserted low at the beginning of clock cycles T3 and T5 (Fig. 3). Command access B(N) and D(P) occur at the same time as the refresh cycles, where T3 or T5 may be seen as the first predetermined time slot, since this is when the command and refresh arbitration will begin. The refresh will occur concurrently with the access request as long as the request does not result in a cache miss (col. 10, lines 60-66; col. 12, lines 27-39). The second predetermined time may be attributed to a time slot after all command accesses have occurred, such as any time after the command D(P). The communication link (command/address bys) as claimed could be any one of a number of signals as detailed

in figure 4. For instance, the WR# or EA[16:0] signals are used for initiating a read or write operation. The controller as claimed refers to the access control (100), which controls operations for the memory array and includes a refresh counter (208) for also controlling refreshing operations (col. 9, lines 19-37). As a result, external accesses can occur concurrently or at a later time without delaying the access command, as recited above.

The difference between the claimed subject matter and that of Leung et al., disclosed supra, is that claims 13, 23, and 56 recite that the first and second predetermined slots are the only time slots during which data access commands may be placed on the bus. Nakajima teaches a system for assigning refresh cycles and memory access cycles according to a designated pattern every refresh cycle (Figure 2; col. 3, lines 15-19 & 31-35). Nakajima also teaches that the data access may be provided every second or third refresh cycle (Figure 3; col. 3, lines 40-47).

Regarding claims 14 and 22, the WR# or EA[16:0] signal lines, as recited above, carry signals related to a read or write operation, which would comprise a command/address bus as claimed for DRAM access.

Regarding claim 17, the refresh controlling operations (as recited above for claims 13, 23, and 56) are part of the access controller as claimed.

Regarding claim 18, refresh timer (195) is used for counting clock cycles and sending a refresh request at a predetermined cycle of every 320 (u)s (col. 10, lines 37-39).

Regarding claim 19, as seen in Figure 4, the refresh commands appear at the same time as the access commands B(N) and D(N) as seen with their corresponding edge placement. The refresh operation is enacted at this predetermined time, and then the arbitration of whether to enact the refresh operation occurs.

Regarding claim 25, the refresh operation occurs concurrently or at a later time cycle as recited above for claims 13, 23, and 56.

Regarding claims 26 and 27, since a command access and refresh operation can exist concurrently should a conflict (cache miss) not occur, the two operations will occur concurrently without delaying the access operation, as recited above for claims 13, 23, and 56.

Regarding claims 28 and 29, Leung et al. teaches that when the access command results in a cache miss (conflict) at the same time of a refresh operation (T5), the access command is allowed to proceed while all DRAM banks except for the DRAM bank corresponding to the command access are allowed to refresh. After the access command has occurred, with the read and write request signals de-asserted high at cycle T6, the refresh command for the DRAM bank related to the access command is allowed to occur at this time (col. 13, lines 26-37, 43-50 and line 62 – col. 14, line 10).

Regarding claims 35, 45, 57, and 58, Leung teaches semiconductor memories using DRAM (col. 1, lines 13-15; col. 2, lines 28-29). Leung does not explicitly state incorporating a processor (claim 45) to control the DRAM memories, but one of ordinary skill in the art would recognize that a processor is inherently required for DRAM

operations to occur. Leung et al. further teaches determining that a refresh cycle is required according to the RFQ# signal being asserted low at the beginning of clock cycles T3 and T5 (Fig. 3). Command access B(N) and D(P) occur at the same time as the refresh cycles, where T3 or T5 may be seen as the first predetermined time slot, since this is when command and refresh arbitration will begin. The refresh will occur concurrently with the access request as long as the request does not result in a cache miss (col. 10, lines 60-66; col. 12, lines 27-39). The second predetermined time slot may be attributed to a time slot after all command accesses have occurred, such as any time after command D(P). The communication link (command/address bus) as claimed could be any one of a number of signals as detailed in figure 4. For instance, the WR# or EA[16:0] signals are used for initiating a read or write operation. The controller as claimed refers to the access control (100), which controls operations for the memory array and includes a refresh counter (208) for also controlling refreshing operations (col. 9, lines 19-37). As a result, external accesses can occur concurrently or at a later time without delaying the access command, as recited above.

The difference between the claimed subject matter and that of Leung et al., disclosed supra, is that claims 35, 45, 57, and 58 recite that the first and second predetermined slots are the only time slots during which data access commands may be placed on the bus. Nakajima teaches a system for assigning refresh cycles and memory access cycles according to a designated pattern every refresh cycle (Figure 2; col. 3, lines 15-19 & 31-35). Nakajima also teaches that the data access may be provided every second or third refresh cycle (Figure 3; col. 3, lines 40-47).

Regarding claims 36, 44, and 54, the WR# or EA[16:0] signal lines, as recited above, carry signals related to a read or write operation, which would comprise a command/address bus as claimed for DRAM access.

Regarding claim 39, the refresh controlling operations (as recited above) is part of the access controller as claimed.

Regarding claim 40, refresh timer (195) is used for counting clock cycles and sending a refresh request at a predetermined cycle of every 320 (u)s (col. 10, lines 37-39).

Regarding claim 41, as seen in Figure 4, the refresh commands appear at the same time as the access commands B(N) and D(N) as seen with their corresponding edge placement. The refresh operation is enacted at this predetermined time, and then the arbitration of whether to enact the refresh operation occurs.

Regarding claims 46, the WR# or EA[16:0] signal lines, as recited above, carry signals related to a read or write operation, which would comprise a command/address bus as claimed for DRAM access.

Regarding claim 49, the refresh operation occurs concurrently or at a later time cycle as recited above for claims 35, 45, 57, and 58.

Regarding claim 50, refresh timer (195) is used for counting clock cycles and sending a refresh request at a predetermined cycle of every 320 (u)s (col. 10, lines 37-39).

Regarding claim 51, as seen in Figure 4, the refresh commands appear at the same time as the access commands B(N) and D(N) as seen with their corresponding edge placement. The refresh operation is enacted at this predetermined time, and then the arbitration of whether to enact the refresh operation occurs.

Allowable Subject Matter

Claims 8-12, 15, 16, 20, 21, 30-34, 37, 38, 42, 43, 47, 48, 52, and 53 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claims 1, 4-23, and 26-58 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is 703-306-5843. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

DS/BRP

Donald Sparks
Supervisory Patent Examiner
Art Unit 2187

March 31, 2004